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(71) Applicant(s)
Ford Motor Company

(Incorporated in USA - Delaware)

County of Wayne, Dearborn, Michigan 48126, United States of America

(72) Inventor(s)
Carl Wilmer Thatcher
Stig Herman Oresjo
John Elliott McDermid
Kenneth P Parker

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(74) Agent and/or Address for Service
A Messulam & Co
24 Broadway, LEIGH-ON-SEA, Essex, SS9 1BN, United Kingdom

(54) **Method and apparatus for testing integrated circuits**

(57) A method and apparatus is disclosed for testing integrated circuit interconnect and measuring the value of passive components interconnecting the IC's (16, 18). Each IC (16, 18) includes both analog (20, 22) and digital circuitry and is provided with a test access port (24, 26) and boundary scan architecture for selectively connecting components to an analog test bus (102, 104) and for testing for the integrity of interconnections. When connected with the test bus (102, 104), a constant current is supplied to the component and the resulting voltage developed across the bus is used for identifying the value of the component. In a second embodiment (Fig 4 not shown) each IC includes a pair of buses (130, 132) which permits measurement of the impedance of the switches connecting the components to the test bus.

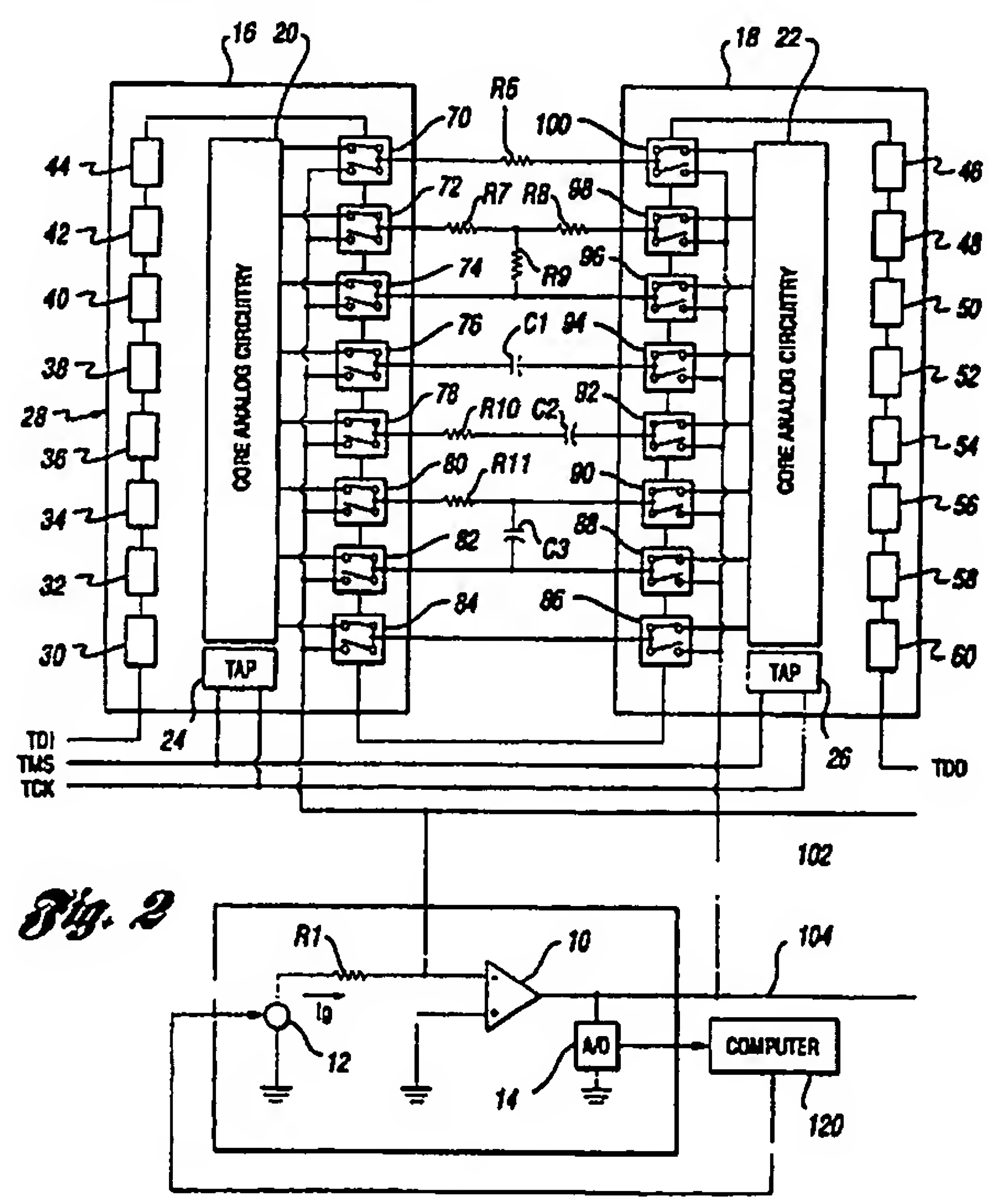

Fig. 2

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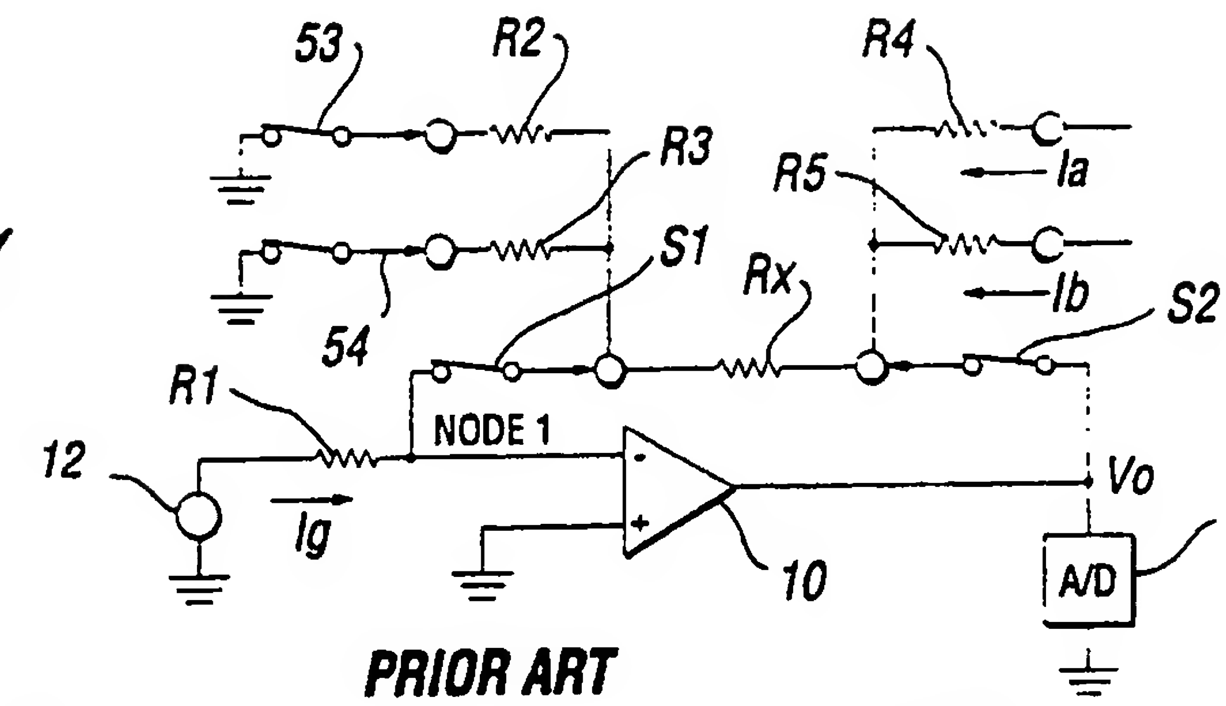
Fig. 1



PRIOR ART

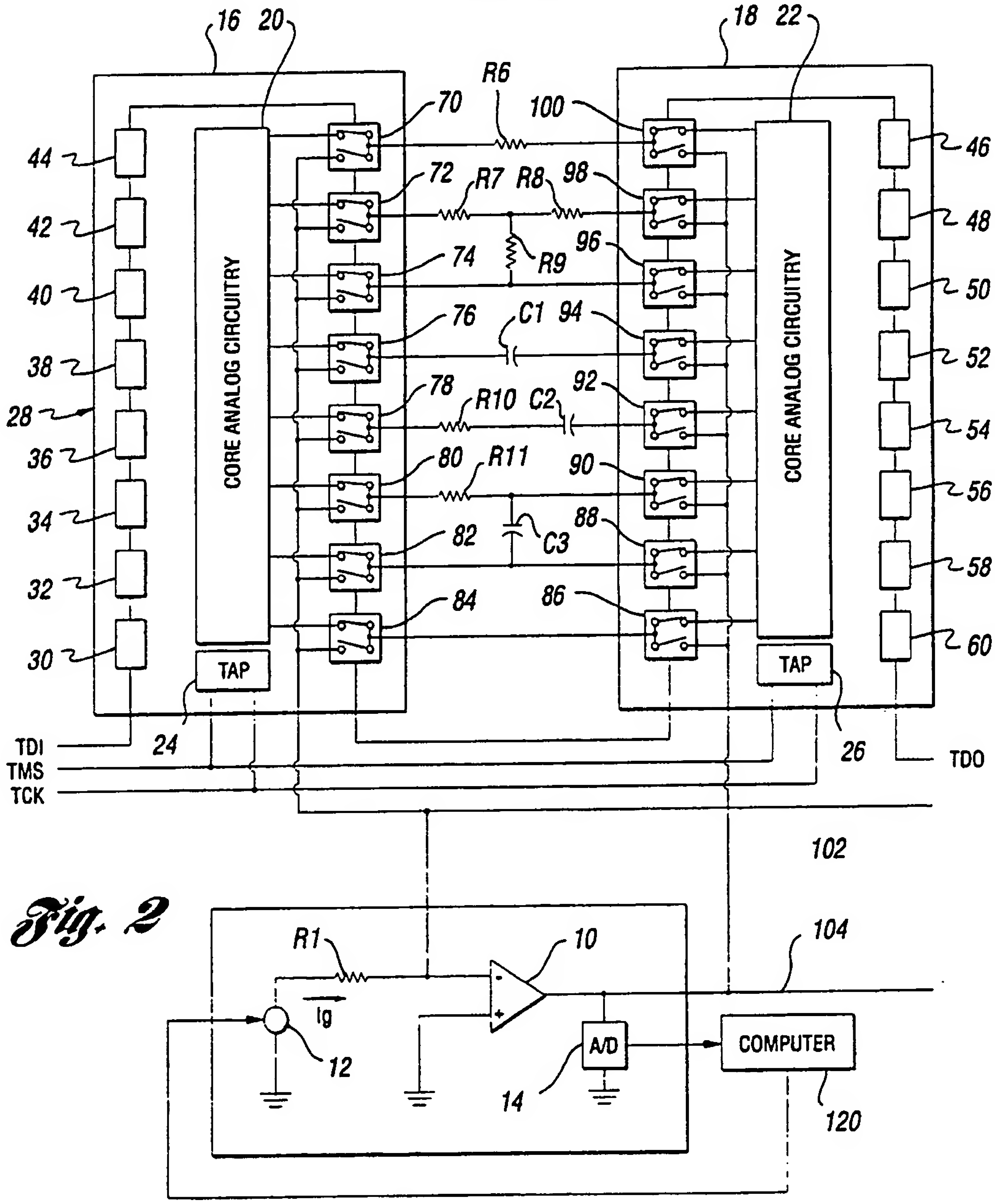


Fig. 2

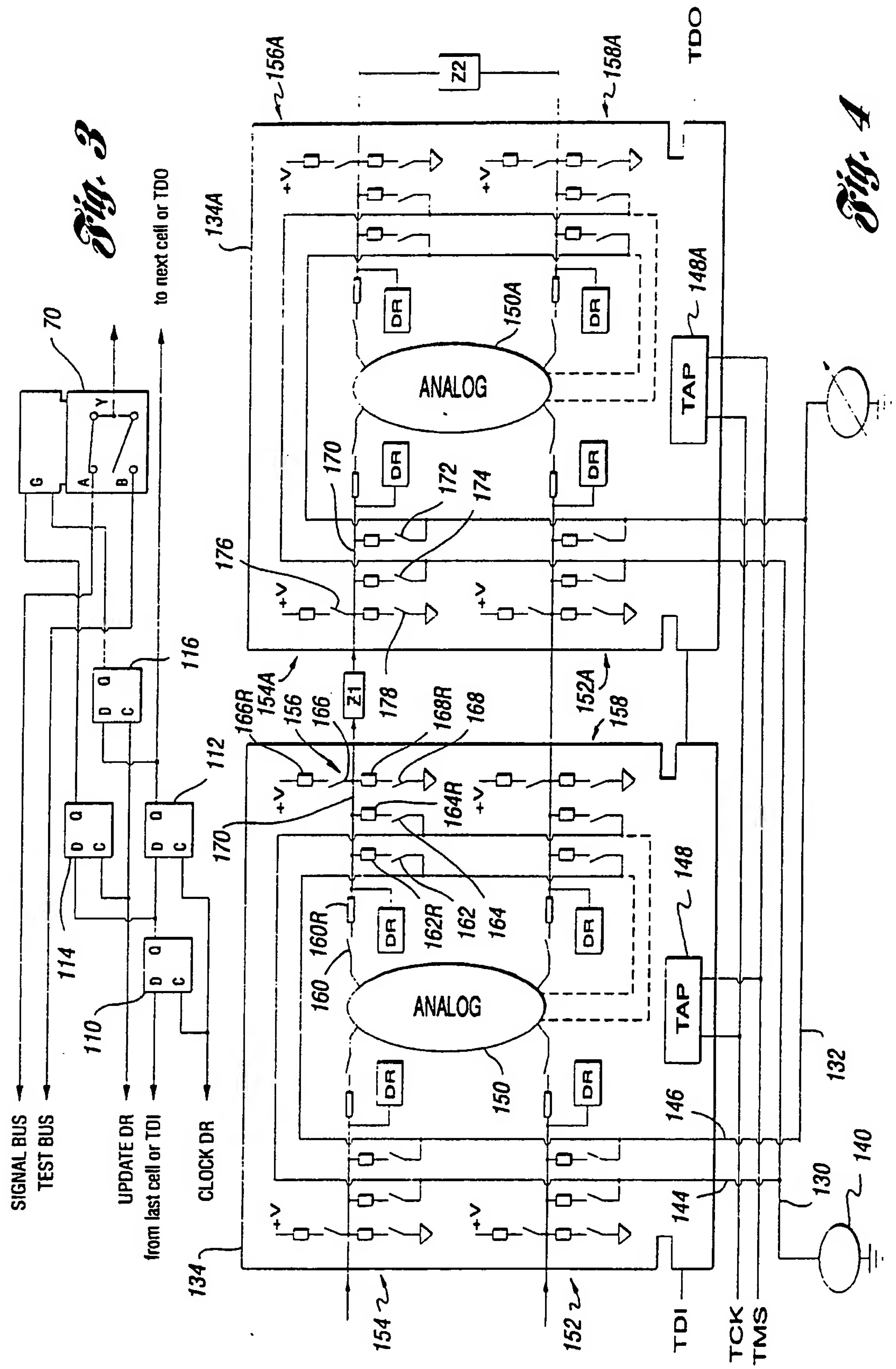


Fig. 3
70
G
A
B
Y
to next cell or TDO
116
D Q C
112
114
110
SIGNAL BUS
TEST BUS
UPDATE DR
from last cell or TDI
CLOCK DR
Fig. 4
156A
158A
TDO
Z2
134A
150A
ANALOG
DR
TAP
148A
170
172
174
176
+V
178
Z1
154A
166R
156
166
168R
168
152A
158
164R
162R
162
164
160R
160
148
150
132
146
144
130
140
134
154
152
TDI
TCK
TMS

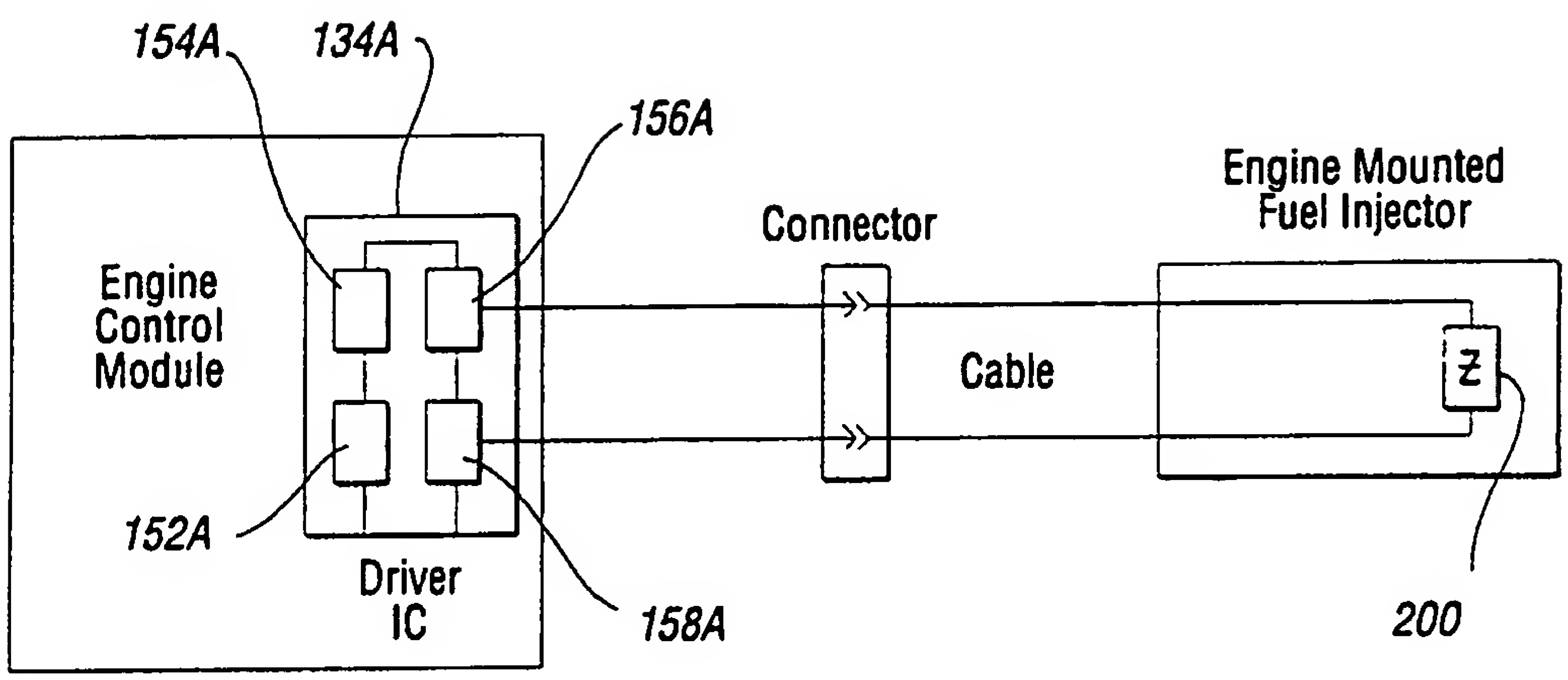

154A
134A
156A
Engine Control Module
Driver IC
152A
158A
Connector
Cable
Engine Mounted Fuel Injector
Z
200

Fig. 5

METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS

This invention relates to a method and apparatus for testing integrated circuits in a mixed signal environment and more particularly to testing interconnects between integrated circuits mounted on printed circuit boards and for measuring the value of electrical components interconnecting the integrated circuits.

A printed circuit board and system level interconnect test is a high priority need in industry. This is particularly so in the automotive industry where many different phases of electronic activity, from IC design to vehicle warranty and customer service, are present and thus involve several areas of testing and diagnostics. At the IC level a significant amount of testing of mixed-signal devices is required. In order to meet the electronic test and diagnostic needs of the automotive industry, the Design-for-Testability (DFT) real estate (both pin count and silicon) must be kept to a minimum in order for the cost to justify the benefits.

The extended period of vehicle warranty requires significant field test and diagnostic capability, and hierarchial testing concepts are required, beginning at the integrated circuit (IC) level and extending to the discrete components on mixed-signal boards and peripheral analog elements in control systems. The increasing trend to integrate greater capability into IC's, resulting in embedded complexities, has significantly reduced the effectiveness of the present in-circuit testing methods at the board level via a "bed of nails" interface. There is therefore a need to provide a "virtual in-circuit" testing at all levels over an analog test bus.

IC, subsystem and system level DFT approaches should entail structures that provide a means for testing for analog drift trends at critical locations within the IC's, PC boards and systems. Data paths to failure under harsh operating conditions are required to establish appropriate

warranty data. Pertinent data feedback over the life of the product to all levels of the process would enhance continuous improvement and project future requirements amidst increasing complexities.

With the foregoing in mind, it is an object of the present invention to provide a method and apparatus for testing interconnects between integrated circuits which exist in a mixed signal environment.

It is a another object of the invention to provide for the measurement of passive components on printed circuit boards which components interconnect analog circuitry on separate IC's mounted on the board, wherein the measurement approach is compatible with boundary scan techniques used in prior art tests of digital integrated circuits.

In accordance with the present invention each IC is provided with multiplex switches for selectively connecting one or more electrical components, such as resistors, capacitors or conductors, either to core analog circuitry in two separate IC's or to a test bus on the IC's. The selection is accomplished by providing a digital test signal which connects the appropriate components to the test bus. In one embodiment each IC includes a single bus. When connected with the test bus, a programmable constant current is supplied to the component and the resulting voltage developed across the bus is used for identifying the value of the component. In a second embodiment each IC includes a pair of buses which permits measurement of the impedance of the multiplex switches providing a more accurate measurement of the component values. Other switches and storage elements are provided on each IC for providing a digital test of the integrity of connections between pins on or between the IC's and for storing the result of the test.

The invention will now be described further, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a diagram of a conventional in-circuit tester;

Figure 2 is a schematic diagram of the present invention applied to a printed circuit board environment;

Figure 3 is a schematic diagram showing greater detail of the switch control circuitry in Figure 2;

Figure 4 is a schematic diagram of a second embodiment of the invention;

Figure 5 is a block diagram showing application of the invention to the automotive system environment.

Referring now to the drawings and initially to Figure 1, a conventional in-circuit tester employed in many manufacturing plants where printed circuit boards are tested, is shown. An operational amplifier 10 having positive and negative inputs amplifies the difference between the two inputs by the gain of the circuit. Both inputs are extremely high impedance, and for most applications, they can be considered infinite in value. The op-amp is used to determine the value of analog components on the printed circuit board.

In the standard in-circuit tester, electro-mechanical switches make up a front-end matrix to interface the amplifier 10 to a probe assembly designed to match the printed circuit nodal pattern. The switches S1 and S2 (in the matrix) are closed as required to sequence each analog component to be tested into the feedback path of the amplifier 10. S3 and S4 (in the matrix) are closed to ground resistors R2 and R3. A constant voltage source 12 is connected with Node 1 through resistor R1. An unknown resistor Rx in the feedback path forms a voltage divider with R1 at Node 1. An analog-to-digital converter 14 measures the output voltage (Vo) of the amplifier 10. With the positive input tied to a reference voltage (ground), the negative input (Node 1) becomes a virtual ground due to the amplifier forcing current through Rx until the voltage

difference across the two inputs is essentially zero. For instance, if the negative input tends to move positive, the output will be amplified in the opposite direction until the potential between the two inputs is essentially zero. If indeed Node 1 is virtual ground, and resistors R2 and R3 have zero potential across them, then all of the current from source 12 (Ig) must go through Rx. The amplifier 10, voltage source 12 and resistore R1 form a constant current source. Since Ig is known and Vo is measured, Rx can be calculated. Excess current from the amplifier 10 (Ia and Ib) go through resistors R4 and R5, but have no effect on the calculation.

Referring now to Figure 2, a portion of the in-circuit tester of Figure 1 is used in accordance with the present invention to test the integrity of the interconnections between a pair of mixed-signal integrated circuits 16 and 18 and to measure passive components such as resistors R6-R11 and capacitors C1-C3, or a conductor 19 between the IC's. These components are mounted on a printed circuit board, which also supports the IC's 16 and 18. The IC's 16 and 18 include core or "mission" analog circuitry 20 and 22 as well as digital circuitry, not shown. A Test Access Port (TAP) control circuitry, generally designated 24 and 26, is provided on each IC 16 and 18 respectively. The TAP's 24 and 26 receive a Test Clock (TCK) and Test Mode Select (TMS) inputs and provide timing outputs, designated UPDATE DR and CLOCK DR in Figure 3, which control a data register generally designated 28.

The register 28 includes eight stages 30-44 contained in IC 16 and eight stages 46-60 contained in IC 18. The data shifted through the register 28 controls multiplex devices 70-100 each of which includes a pair of switches. The devices 70-84 selectively connect the aforementioned passive board mounted components either to the input/output conductors of the analog circuitry 20, or to a test bus 102, a portion of which is contained within the IC 16 but accessible through a pin of the IC 16. Similarly, the devices 86-100 selectively connect the components either to

the input/output conductors of the circuitry 22 or to a test bus 104. The position of the switches in the devices 70-100 is determined by a test vector or data word that is shifted in the register 28 via a Test Data In (TDI) line and shifted out via a Test Data Out (TDO) line all under the control of the TAP control circuitry 24 and 26. Node 1 at the negative input of the operational amplifier 10 is connected with the test bus 102 and the output of the amplifier 10 is connected with the test bus 104. When at least one of the devices 70-84 and one of the devices 86-100 is placed in a test mode position, a constant current from the generator 12 is fed through the closed switches to one or more of the passive components on the circuit board. The analog voltage developed at the output of the amplifier 10 is converted by the A/D converter 14 and fed to a computer 120 for determining the value of the component(s). The computer 120 also controls the programmable generator 12 to set the desired current level.

With reference to Figure 3, each of the multiplex devices 70-100 may contain D-type flip-flops 110-116. The test vector is shifted through the register 28 and the flip-flop 110 and 112 in each multiplex devices. At any particular point in time one of four binary data pairs, 00,01,10, and 11 appear at the Q outputs of the flip-flops 110 and 112. When the desired test vector has been serially loaded, the UPDATE DR signal shifts the data at the Q outputs of the F/F's 110, 112 to the F/F's 114 and 116 respectively. The latched outputs of the F/F's control the gates of two FET switches respectively, to thereby select either the signal bus to the circuits 20 and 22 or the test buses 102 and 104.

There are significant differences between the on-board test IC of Figure 2 and the external in-circuit tester shown on Figure 1. Some of these differences are as follows: 1) The on-board test op-amp will not be powered by two power supplies, one for the positive voltage, and the other for the negative voltage. Instead, a protected voltage source derived from the vehicle battery (+V) would provide for

both. 2) The positive input to the op-amp, stimuli and voltage measuring circuit could be referenced to a voltage equal to +V/2. 3) The switching matrix, probe assembly, interconnect wiring and associated control software in the in-circuit tester are no longer needed for the simpler IC integrated approach. This will reduce the cost of future testers.

Referring now to Figure 4, a second embodiment of the invention is shown. In this embodiment an analog bus having input and output lines 130 and 132 respectively extend within each of the plurality of IC's 134, and 134A mounted on the printed circuit board. The additional bus on each IC adds an additional pin over the embodiment of Figure 2, but provides offsetting advantages in accuracy of measurement of components, where the impedance of the multiplex switches is large. In order to conserve silicon real estate, the multiplex switches may be located on the IC so that relatively small amounts of silicon are used which will necessarily result in higher switch impedance values.

A current source generally designated 140 is connected with the bus 130 and a voltage detector generally designated 142 is connected with the bus 132. Alternatively, the source 140 could be a constant voltage source and the detector 142 would then be a current detector. The IC 134 includes conductors 144 and 146 which connect with the buses 130 and 132 respectively and to a plurality of switches. These switches are actuable to either an open or closed position under the control of test circuitry in a Test Access Port (TAP) 148 as previously discussed. The control circuitry includes a boundary-scan register (not shown) as is well known in the art and includes a standard interface providing instructions for control of the switches. In Figure 4, for purposes of illustration, each IC includes four groups of switches generally designated 152-158, and 152A-158A respectively. In the interest of brevity only group 156 will be discussed in detail. The switch group 156 includes switches 160-168. Associated with each switch is an internal impedance designated by the suffix "R". The

switch 160 is actuable to connect or disconnect the analog circuit 150 with a conductor 170 connected with an input pin of the IC 134. When a test mode is selected the switch 160 is opened. The switch may be contained within the analog circuit 150. For example, the function performed by the switch 160 may be performed by turning off the output driver of an operational amplifier forming a part of the circuit 150. In that case, it would be the responsibility of the IC designer to fabricate the appropriate level of control from the boundary scan test word. The switches 164 and 166 connect the conductor 170 to the bus 130 and 132 through the conductors 144 and 146 respectively. The switches 166 and 168 are connected with an IC operating voltage and ground respectively, and are provided to simulate the IEEE Standard 1149.1 EXTEST in a mixed-signal environment. EXTEST is a connectivity test procedure for testing digital integrated circuits. Further details regarding EXTEST as well as background information may be had from the IEEE Standard Test Access Port and Boundary-Scan Architecture published by the IEEE, May 21, 1990. While not shown in Figure 4, it will be understood that the IC's contain digital as well as analog circuits. Control of the switches 166 and 168 will for example permit the detection of a cross family short between an IC pin connected with analog circuitry and an IC pin connected with digital circuitry. By selective closure of the switches to +V or to ground a digital "1" or "0" can be generated and then detected by a data register which includes a stage DR, associated with each switch group.

By selective closure of the appropriate switches in the switch groups in IC's 134, and 134A, the component Z1 can be connected with the constant current source 140 and appropriate measurements can be made by the detector 142 in order to determine the impedance of the component(s). Considering, for example, the component Z1 and the switch group 156 in IC 134 and switch group 154A in IC 134A, the switch 164 is closed to connect one side of Z1 to the current source 140 and switch 178A is closed to connect the other side of Z1 to ground. The value of Z1 is determined

by connecting the voltage detector 142 to the left side of Z1, by closure of switch 162, and measuring a voltage V_3, then opening the switch 162 and closing the switch 172A, connecting the voltage detector 142 to the right side of Z1 and measuring a voltage V_4. The value of Z1 is then the difference between the voltage measurements V_3 and V_4 divided by the constant current. Any switch impedance in series with Z1 will change V_3 or V_4 but not the difference V_3-V_4.

The dotted line extensions of the conductors 144 and 146 in IC 134, as well as the corresponding conductors in the IC 134A, are intended to indicate that, if desired, measurement can be made within the analog circuit 150.

Figure 5 shows the test bus extending beyond the control module board level into a typical sub-system such as an engine control module and to sensors or actuators connected with the module and existing in a harsh environments. In the automotive electronic industry, a control module interfaces with many peripheral sensors for monitoring the many variations of conditions through which the system must operate. For example, in the engine control system the air-fuel ratio must be at the right mixture under all atmospheric conditions, whether it be for temperature, moisture, altitude, etc. Many actuators are involved to meter the fuel, adjust the spark timing, re-circulate crankcase fumes, etc. to assure quality operating vehicles. Drift in impedance through the interconnecting circuitry cannot be ignored. The harsh operating environments of temperature extremes, temperature cycles, anti-freeze spills, road salts, etc., all effect the aging process. The many interconnections making up the system must be measured for analog changes. The common trial and error practices of replacing a sensor or actuator, disconnecting cables for test, etc., masks many real conditions producing failures, and destroy any hope of identifying the failure mechanisms in the natural setting. In Figure 5, the value of an electrical component forming an actuator 200 driven by IC 134A, can be measured using the approach shown in Figure 4.

The switch groups 156A and 158A can be selectively closed in order to connect the sensor 200 with the constant current source such as 140 of Figure 4 and then voltage measurements on either side of the sensor are made using a voltage detector such as 142 of Figure 4.

CLAIMS

1. Apparatus for measuring electrical component means interconnecting first and second integrated circuit devices which devices include first and second analog circuits respectively, said apparatus comprising a first and a second analog test bus means included in said first and second devices respectively, multiplex means included in each of said devices for selectively connecting said component means either to said analog circuit means or to said analog test bus means, test circuit means connected with said first and second test bus means and including a source for supplying a current to said component means when said component means is connected with said test bus means and detector means for determining the value of said component means.

2. Apparatus as claimed in Claim 1, wherein each of said devices further including switch means for selectively connecting a pin of the device with a voltage source or a reference voltage, each of said devices including storage means for storing a digital 1 or 0 for indicating the integrity of the interconnection between said pin and one or more other pins on said devices.

3. Apparatus as claimed in Claim 1, wherein said constant current is supplied by a programmable constant current generator and said voltage is measured by an analog to digital converter.

4. Apparatus as claimed in Claim 3, wherein said constant current source includes an operational amplifier, means connecting one input of the amplifier to a reference voltage, resistor means connecting a second input of said amplifier to a constant voltage source, means connecting a node between said resistor means and said second input of said amplifier to said first test bus, means connecting the output of said amplifier to said second test bus, said converter means converting the analog voltage developed

across said first and second test buses to a digital value, and computer means for determining said selected component value based on said digital value.

5. Apparatus as claimed in Claim 1, wherein said electrical component means includes a plurality of passive components, said first and second analog circuits each including a plurality of input/output conductors, said first and second switch means each including a plurality of pairs of switches, one of each pair of said pairs of switches adapted to connect said components with said input/output conductors to establish a predetermined circuit configuration between said first and second analog circuits, the other of each pair of said pairs of switches adapted to connect one or more of said components across said first and second test buses.

6. Apparatus as claimed in Claim 5, wherein said multiplex means includes switch control means, said switch control means including a plurality of storage elements for selectively activating said pairs of semiconductor switches in accordance with a digital test vector.

7. Apparatus as claimed in Claim 6, wherein each of said storage elements includes at least a first and second flip flops for controlling respective switches in said pairs of switches.

8. A method of measuring the value of an electrical component interconnecting analog circuitry located on first and second integrated circuit devices and comprising the steps of:

a. selecting the component for measurement by disconnecting the component from said analog circuitry and connecting the component to a test bus and loading an appropriate digital test vector in memory means located on each of said devices,

b. passing a constant current through the selected component, over an analog bus including at least one conductor and a switch located on each device and measuring the voltage developed across said conductors on said devices,

c. determining the component value between said devices using the voltage measured in step b.

9. A method as claimed in Claim 8, wherein each analog bus includes a pair of conductors and a pair of switches located on each device and wherein said step b. includes passing the current over one of the pair of conductors and one of the pair of switches on each device in one direction through said component, passing the current over the other of the pair of conductors and the other of the pair of switches in the opposite direction through said component, and passing the current through the pair of switches on one device and then the other device.

10. Apparatus as claimed in Claim 1, wherein each of said first and second analog test bus means includes a single conductor on each of said devices, the conductor on said first device connected with said source and the conductor on said second device connected with said detector means.

11. Apparatus as claimed in Claim 1, wherein each of said first and second analog test bus means includes a pair of conductor on each of said devices, one of each of said pair of conductors connected with said source and the other of each of said pair of conductors connected with said detector means.

12. Apparatus as claimed in Claim 11, wherein each of said devices includes at least first and second switches adapted to be concurrently closed and placed in series across said pair of conductors whereby the impedance of said first and second switches can be measured.

13. Apparatus as claimed in Claim 12, wherein each of said devices includes an internal conductor connected to one side of each of said first and second switches, the other side of one of said switches connected with said source, the other side of the other of said switches connected with said detector.

14. Apparatus as claimed in Claim 13, wherein each of said devices includes a third switch connected between said internal conductor and a voltage source for the device and a fourth switch connected between said internal conductor and ground, said internal conductor being connected with a pin of said device, a storage element connected with said internal conductor for storing the logic level on said internal conductor when said third or fourth switch is closed.

15. A method of measuring the value of one of a plurality of electrical components interconnecting analog circuitry located on first and second integrated circuit devices and for testing the integrity of the interconnection between said devices, comprising the steps of:

a. selecting a component by loading an appropriate digital test vector in memory means located on each of said devices,

b. passing a constant current through the selected component and measuring the voltage developed across said selected component,

c. determining the component value or the integrity of interconnection between said devices using the voltage measured in step b.

16. Apparatus for testing integrated circuits substantially as herein before described with reference to figures 2 to 5 of the accompanying drawings.

17. A method for testing integrated circuits substantially as herein before described with reference to figures 2 to 5 of the accompanying drawings.

Patents Act 1977 **Examiner's report to the Comptroller under Section 17** **(The Search report)** 15	Application number GB 9409164.2
Relevant Technical Fields (i) UK Cl (Ed.M) G1U (VR3128 AND VR3130) (ii) Int Cl (Ed.5) G01R (31/28, 31/30 AND 31/302)	Search Examiner KEN LONG Date of completion of Search 4 AUGUST 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) NONE	Documents considered relevant following a search in respect of Claims :- 1 TO 17

Categories of documents

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Category	Identity of document and relevant passages		Relevant to claim(s)
A	GB 2180355 A	(N V PHILIPS) see particularly page 1 lines 69 to 72 and 81 to 108	
A	GB 2157837 A	(MARS) see particularly page 1 lines 5 to 12 and 69 to 101	
A	US 5070296	(HONEYWELL) see particularly column 2 lines 28 to 49	

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